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# DESIGN OF A FAST GATED CHARGE INTEGRATING FRONT END FOR USE IN HIGH DENSITY CAMAC AND FASTBUS MODULES

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This paper describes the design principles of two versions of a gated charge integrating front end for use with high energy physics particle detectors. The current integration, gate and clear problems are discussed. A high slew rate design and its implementation on a very small printed circuit board is presented. The design of a 32 channel, 12 bit CAMAC charge integrating ADC is outlined.

## 1. Introduction

Electronic detectors used for particle identification purposes in high energy physics (HEP) experiments produce current signals of variable amplitude, shape and width. The electric charge contained in each pulse must be digitized so that it can be used for processing in large computer systems.

Over the last ten years detectors have been increasing in size and number of channels thus placing severe constraints on the cost per channel of the electronics while requiring higher resolution and dynamic range. Future CERN-LEP experiments [1–4] will use about 500 thousand charge digitizers which must typically have a 12 bit resolution over a 15 bit dynamic range for pulses with slew rates as high as 2 mA/ns. A recent compilation of existing charge integrating analog to digital converters (ADCs) suggested the authors that a cheap, small front end might be designed without requiring the use of integrated or even hybrid circuit techniques. The two circuits briefly described in this paper integrate the detector current for the duration of a gate pulse. The charge is stored in a capacitor which can then either be fast cleared or digitized by a conventional voltage ADC within two milliseconds.

The 12 bit resolution has been easily achieved with both circuits and 15 bit dynamic range operation with a 32 channel CAMAC unit will be evaluated next summer at CERN on a test module of the OPAL [4] barrel lead–glass electromagnetic calorimeter.

## 2. Survey of electric charge digitization techniques

High accuracy charge integrating ADCs differ in the way they digitize the charge stored in the front end capacitor.

In the well known Wilkinson, or run down, ADC technique the capacitor is discharged with a small constant current and the discharge time is measured with a conventional clock/counter circuit [5]. The input charge-to-discharge time ratio is thus independent of the capacitor drift with time and temperature. However, the number of components per channel is high and this type of front end will progressively disappear in HEP experiments.

Fast and low ON resistance DMOS FET switches, faster and better J FET and MOS FET operational amplifiers, analog multiplexers and cheaper high accuracy successive approximation ADCs have been available since 1976. As a result multiplexed systems [6,7], where the charge stored into 32 or more capacitors are sequentially routed to the input of a single ADC, can be designed. Two techniques are used to route the charge. They are:

(a) the voltage bus;

(b) the current bus.

The second one has been introduced in 1982 by a well known manufacturer [8] and it has not yet been thoroughly evaluated. It is however felt by the authors that the two methods give similar results.

In the first technique the potential on the capacitor terminal is switched through a buffer amplifier onto a common voltage bus driving the ADC. In the second method, the capacitor is switched and discharged into a common charge integrating buffer via the current bus. The voltage at the output of the charge integrating buffer is then measured with a conventional ADC.

Both techniques require a good charge integrate and hold front end and a stable capacitor. Drifts and nonlinearities of the front end were in the past corrected by a processor which was continuously monitoring the performance of the system. The two discrete components designs described in this paper utilize a stable

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capacitor and they are linear over the whole dynamic range; monitoring and calibration are therefore kept to the minimum (i.e. pedestal and gain measurement). Moreover, the capacitor value can be chosen between 100 pF and 620 pF thus allowing for various input sensitivities.

## 3. Design principles of the proposed gated charge integrate and hold circuits

A schematic of the circuit is shown in fig. 1. The switch SW is closed for the duration of the gate pulse thus charging the capacitor $C_I$ with a current $I_0$ proportional to the input current $I_{in}$. Outside the gate pulse the switches SW and CSW are open and the capacitor $C_I$ is isolated thus holding a voltage

$$V = \frac{1}{C_I}\int_0^{t_{gate}} I_0(t)\,dt.$$

This voltage is buffered by a voltage follower A1 that drives the input of a MOS multiplexer (not shown). The charge integrated into the $C_I$ capacitor can then be cleared at any time via the CSW switch.

The $I_0$ current can either be the input current $I_{in}$ or some fraction of it (e.g., common base bipolar input with or without multiemitters, current mirrors etc.).

### 3.1. The input current-to-current converter

Three current-to-current converters are shown in fig. 2 for a negative input current $I_{in}$. They use a differential amplifier A and a transconductance component (bipolar transistor, MOS FET, J FET etc.) thus creating a virtual ground at the input terminal.

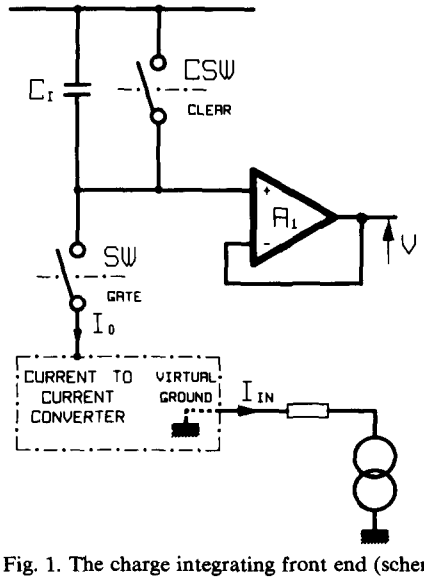


Fig. 1. The charge integrating front end (schematics).

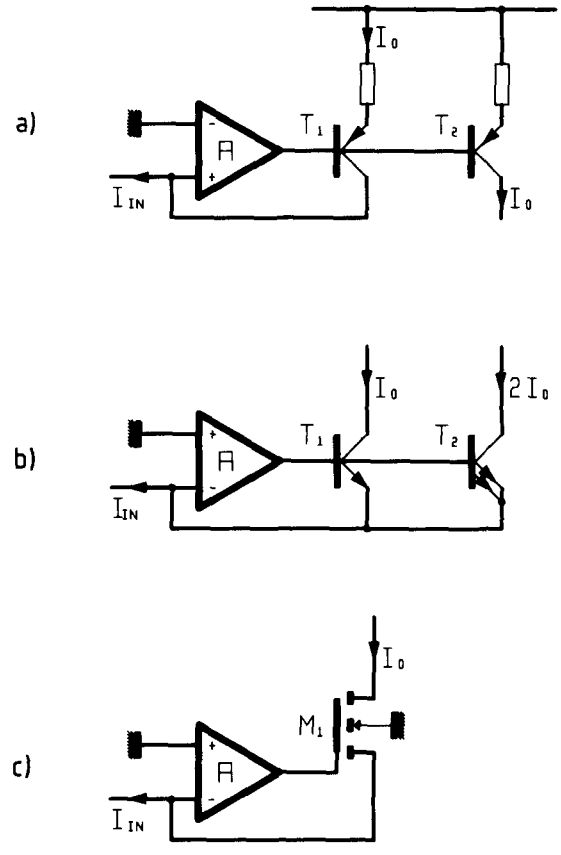


Fig. 2. Three current-to-current converter circuits with virtual ground input.

The circuit in fig. 2(a) is often used to generate weighted currents in digital to analog converters (DAC). The current $I_0$ is available either in the emitter of $T_1$ or in the collector of the "mirror" transistor $T_2$. $I_0$ is equal to $I_{in}$ if one neglects the base currents of $T_1$ and $T_2$.

The circuit in fig. 2(b) is referred to in the nuclear electronics literature [9] as the FEEDBY circuit. The sum of the collector currents following in $T_1$ and $T_2$ is equal to $I_{in}$ again neglecting the base currents of $T_1$ and $T_2$.

The circuit in fig. 2(c) is a MOS FET version of the previous two. In this last circuit, the $I_0$ current is equal to the input current $I_{in}$.

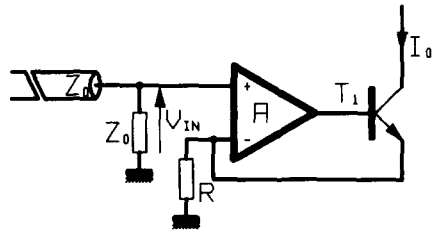


Fig. 3. Positive voltage to negative current converter circuit.

These three circuits can also be used for voltage-to-current conversion as shown in fig. 3 where

$I_0 = V_{in}/R$.

### 3.2. The gate and clear circuits

Three MOS FETs SW1, SW2 and CSW are used as shown in fig. 4(a). The timing diagram in fig. 4(b) shows a complete CLEAR, INTEGRATE, HOLD and CLEAR sequence.

The rest, CSW and SW2 are closed (conductive!) while SW1 is in a high impedance state. $C_I$ is therefore grounded and there is soon no current flowing into CSW.

The CLEAR signal must be removed just before the beginning of the gate pulse during which SW1 is closed while CSW and SW2 are open. The current $I_0$ is then flowing into the $C_I$ capacitor thus integrating $I_0(t)$ for the duration of the gate pulse.

At the end of the gate pulse SW1 is opened and SW2 closed thus leaving $C_I$ in a HOLD state and connected to the input of the voltage follower $A_1$.

The output of the voltage follower can then be routed through a multiplexer to the ADC input for digitization. As soon as analog-to-digital conversion has completed, CSW can be closed thus clearing the charge stored in $C_I$.

It is readily seen that SW1, SW2 and CSW must be as close as possible to ideal switches. DMOS FETs with their low ON resistance ($\sim 50\ \Omega$) and their low inter-electrodes capacitances are ideally suited to this type of application. Feedthrough charges injected by the gate and clear signals are very small and may be partly cancelled with a neutralization capacitor connected to the complement of the clear signal.

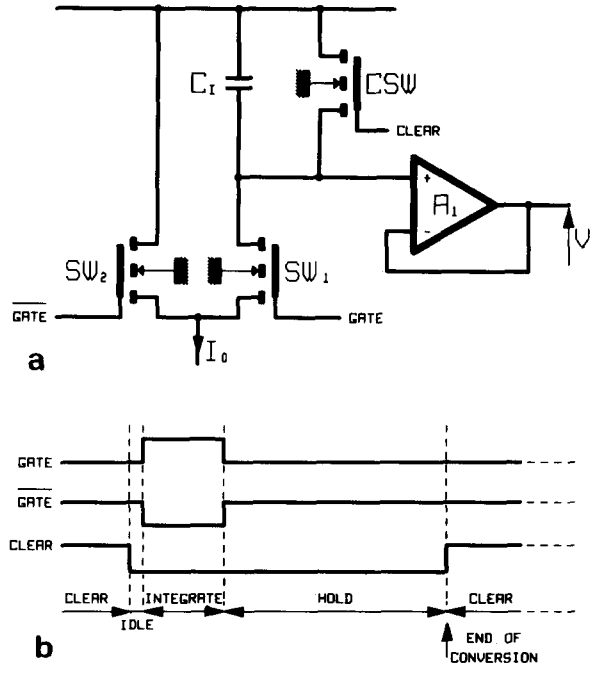


Fig. 4. The gate and clear circuits as shown in (a) operate according to the timing diagram in (b).

The clear function may also be implemented with SW1 and SW2 only. It is then necessary to turn them ON simultaneously during the CLEAR phase. This technique is however not used in the two designs described below.

The gate and clear circuits are identical for the two charge integrating front ends described in the next sections.

## 4. Circuit design and performance with a DMOS FET front end

### 4.1. Description

A detailed schematic of the circuit is shown in fig. 5. The input current-to-current converter is based on the circuit shown in fig. 2(c). The gate and clear circuits are those described in the previous section.

The input amplifier A is a long tail pair of bipolar transistors $T_1$, $T_2$ with a 7.2 mA current source: $T_3$. A 3.6 mA current source in the collector of $T_1$ gives this circuit a very high open loop gain thus ensuring a good virtual ground at the input.

$T_1$, $T_2$ and $T_3$ are half a CA3102 E [10] bipolar amplifier array. The feedback DMOS FET $M_1$ is a quarter of a Siliconix SD 5000N [11,12] the remaining FETs in this integrated circuit being used for the gate and clear circuits.

The $R_p$ resistor between the virtual ground input and the $-12$ V line defines a minimum bias current through $M_1$ and either of the gate switches. This current is integrated during the gate and contributes to the pedestal but it is required to:

(a) improve the low and non-linear transconductance of $M_1$ for very low input currents;

(b) have a minimum gate–source voltage on $M_1$ so that the collector–base voltage of $T_1$ is sufficiently high to ensure a minimum amplification;

(c) linearly process small positive current $I_{in}^{+} < I_{R_p}$.

The charge integrating capacitor $C_I$, 620 pF 1%, has a polystyrene dielectric. It has therefore very low leakage, a high stability and it does not exhibit any memory effect. The 1% accuracy ensures a low gain dispersion from channel to channel.

The voltage follower $A_1$ has a FET input thus limiting the discharge of $C_I$ during the HOLD. Two operational amplifiers have been successfully used for this purpose:

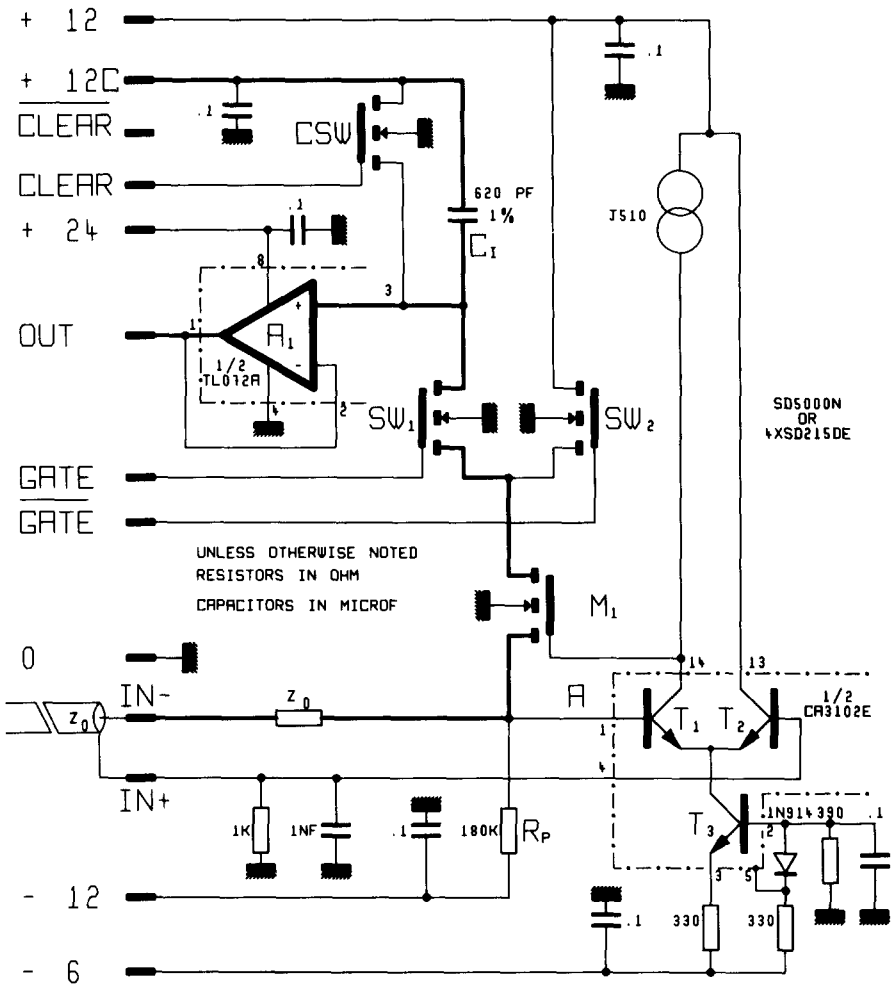


Fig. 5. Detailed diagram of the gated charge integrating front end with a DMOS FET input current-to-current converter.

(a) TL 072 [13] or equivalent, a J FET type;
(b) CA 082 [10], a MOS FET type.

### 4.2. Performance

#### 4.2.1. Linearity

It strongly depends on the stability of the virtual ground at the input of the circuit. In most cases the detector current source is connected through meters of transmission line (coaxial or twisted pair cables) and it behaves as a voltage generator driving the circuit through typically $2 \times 50\ \Omega$ resistors in series (characteristic impedance of the cable plus terminating resistor). Therefore, variations of the voltage level at the virtual ground terminal will introduce non-linearities in the charge integration.

The current flowing into the front end (and the $C_I$ capacitor) depends on the value of the equivalent resistor seen from the virtual ground

$$R_{in} \simeq 1/(g_m A),$$

where $g_m$ is the transconductance of the $M_1$ FET and $A$ the open loop gain of the long tail pair. For small signals $R_{in}$ is fairly small whereas for large signals the amplifier slew rate limits the feedback action thus introducing non linearities.

However, this circuit remains linear for input slew rates as high as 1 mA/ns.

#### 4.2.2. Gate and clear circuits

The signals at the gate and $\overline{\text{gate}}$ terminals must have a 6 V swing (+16 V; +10 V) with rise and fall times shorter than 10 ns. Gate widths as short as 50 ns can be used without any loss in linearity or stability.

The fast clear time depends on the ON resistance of the DMOS FET hence on its gate source voltage $V_{GS}$.

For $V_{GS} = 8$ V, $R_{ON} = 45\ \Omega$, $C_I = 620$ pF. The decay time constant $R_{ON}C_I = t \simeq 30$ ns and $C_I$ is cleared after a time $t_c \simeq 10 \times t = 300$ ns.

*4.2.3. The hold*

The maximum hold time not only depends on the bias and leakage currents but also on the printed circuit board layout. Losses as low as 1 mV/ms have been achieved thus allowing for a minimum of 32 digitizations per ms (32 channels per successive approximation ADC).

*4.3. Evaluation prototype*

The front end described in this paragraph has been laid on a 10 mm × 52 mm printed circuit board (fig. 6) and 16 of such cards were plugged into a CAMAC mother board equipped with a 16 channel multiplexer type AD 7506 and a 12 bit AD 574A successive approximation ADC [14].

The specifications of this module are given in table 1.

The module was extensively tested with a mercury relay pulse generator and proved to be very linear and stable as shown by the histograms in fig. 7.

However, the circuit exhibits non-linearities whenever the input slew rate exceeds 1 mA/ns.

Table 1

| | |
|---|---|
| Input sensing | Charge, direct current integrating |
| Full scale | 800 pC |
| Gain | Typically 5 counts/pC for a 12 bit ADC |
| Input impedance | 50 Ω ± 5%; 0 to 30 mA DC |
| Input limitations | Maximum voltage for linear response: −1.5 V, +20 mV, maximum slew rate for linear response: 2 mA/ns |
| Integral linearity | Within ±0, 4 pC of the best straight line |
| Residual pedestal | Typically 40 pC for a gate width of 200 ns and high source impedance |
| Pedestal/gate width coefficient | Typically 8 pC per 100 ns |
| Stability | See fig. 7 |
| Gate input | NIM: −16 mA into 50 Ω |
| Gate width | ≧ 50 ns |
| Gate timing | The gate signal must precede the analog inputs by ≧ 50 ns |
| Fast clear | NIM: −16 mA into 50 Ω; width: ≧ 15 ns; settles to within 1 count in ≧ 200 ns |

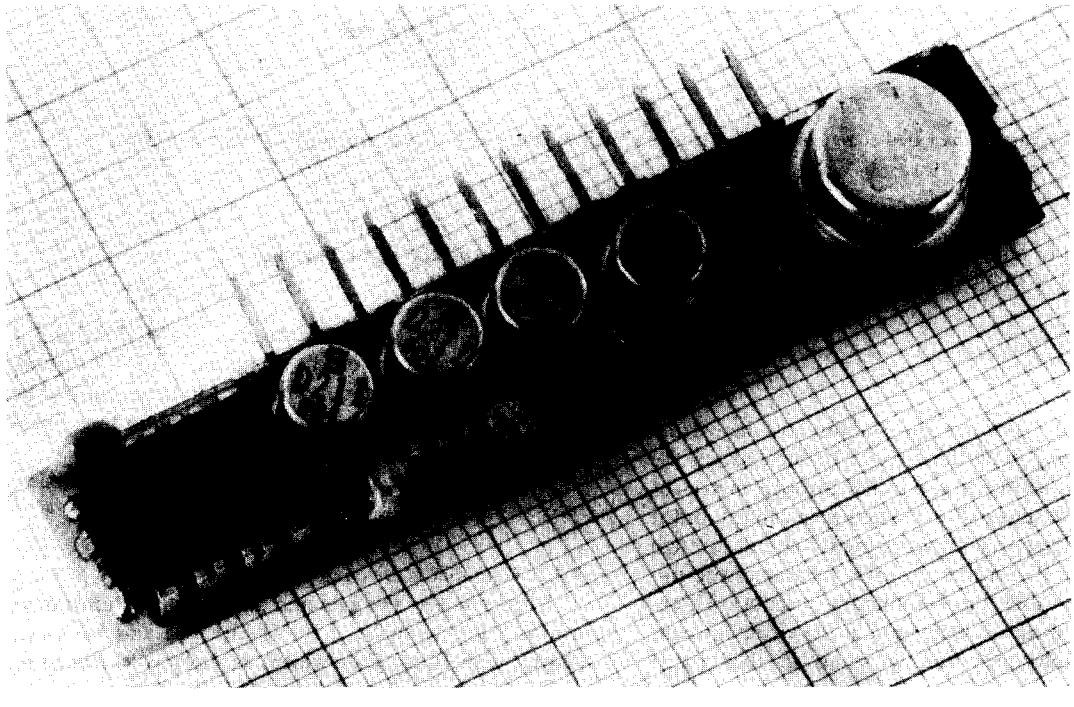

Fig. 6. Photograph of a single channel circuit; individual DMOS FETs (SD 211) are used instead of the SD 5000 array mentioned in the text.

```
HISTOGRAM # 1  ADC STABILITY
TOTAL  = 1000.   UNDER  = 0.  OVER = 0.
MEAN   = 225.367  R.M.S. = .484057
                0                                                    634
BIN  CONTENTS  ------------------------------------------------------------
220    0       I
221    0       I
222    0       I
223    0       I
224    634     I****************************************************************
225    365     I**********************************
226    1       I
227    0       I
228    0       I
229    0       I
```

```
HISTOGRAM # 1  ADC STABILITY
TOTAL  = 1000.   UNDER  = 0.  OVER = 0.
MEAN   = 2942.94  R.M.S. = .22798
                0                                                    945
BIN  CONTENTS  ------------------------------------------------------------
2937   0       I
2938   0       I
2939   0       I
2940   0       I
2941   55      I***
2942   945     I****************************************************************
2943   0       I
2944   0       I
2945   0       I
2946   0       I
```

Fig. 7. Histograms of pedestal and 3/4 full scale data showing the very good circuit performance for a 12 bit dynamic range.

## 5. A high slew rate version using bipolar transistors

### 5.1. Description

Bipolar transistors have a higher transconductance $g_m$ than FETs, it can therefore be seen that the circuit in fig. 2(a) has a lower input resistance at the virtual ground terminal than the one described in the previous paragraph.

The detailed schematic of this second charge integrating front end is given in fig. 8. The M1 FET has been replaced by a bipolar pnp transistor driven from the collector of $T_2$. Two poles are thus introduced in the amplifier and the circuit may oscillate. A small feedback capacitor $C_s$ between the collector and the base of $T_1$ stabilizes the circuit.

### 5.2. Performance

This charge integrating front end is superior to the one described in sec. 4. It is linear for input pulses with a 2 mA/ns slew rate if the $T_4$ transistor has an $f_T$ greater than 500 MHz for a 10 mA collector current. The MPS 3640 and the 2N 3546 transistors [15] have been successfully used in this circuit.

The stabilizing capacitor $C_s$ does not affect the circuit performance, it is a 12 pF ceramic one.

The specifications of the circuit are identical to those given in table 1 except for the slew rate which is at least 2 mA/ns.

### 5.3. Printed circuit board layout

Two channels have been laid on a 21 mm × 42 mm printed circuit board equipped with a 16 pin dual-in-line (DIL) connector (fig. 9). The overall thickness is less than 8 mm and the device can be housed in a single width CAMAC module.

The bases of the $T_1$ and $T_2$ transistors are accessible on the DIL connector and the circuit can be used as a "quasi-differential" device i.e.:

(a) base of $T_2$ connected to the input cable ground for the integration of negative currents with a good signal to pick up noise ratio;

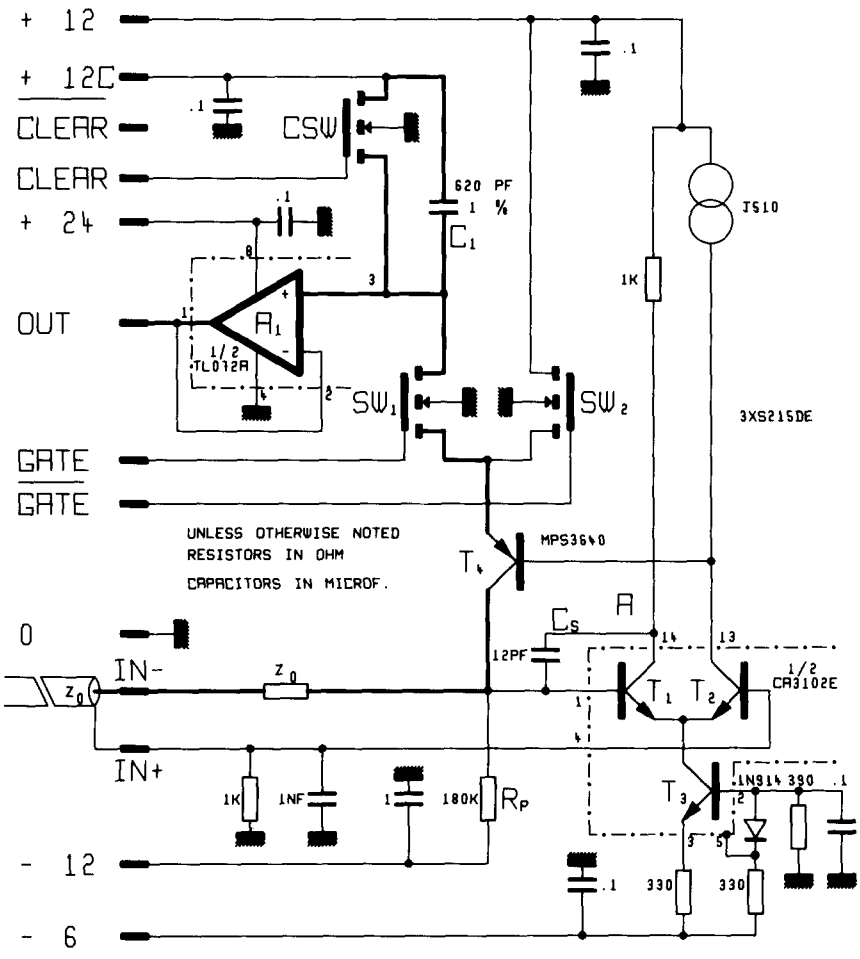


Fig. 8. Detailed diagram of the high slew rate circuit.

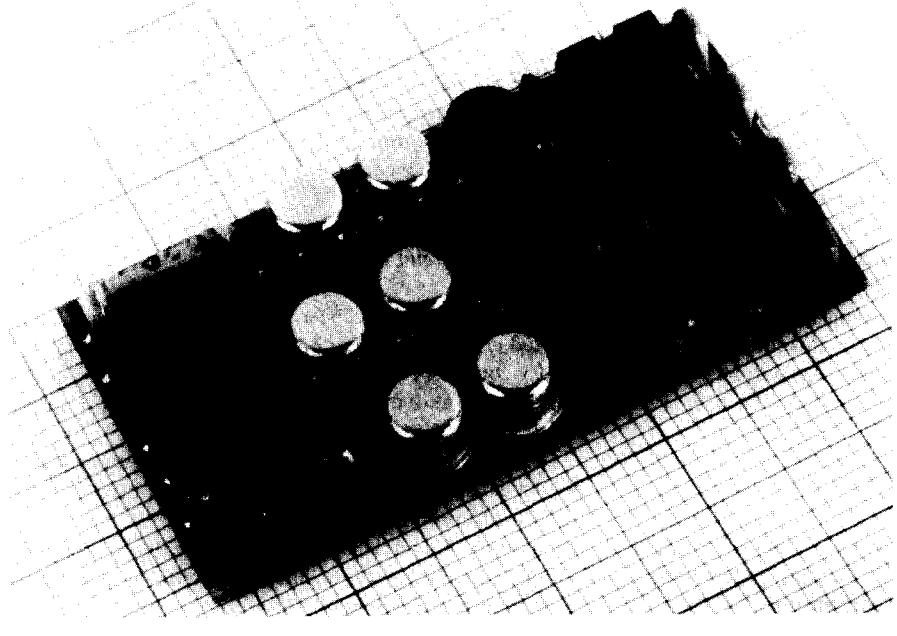

Fig. 9. Photograph of a dual channel circuit; its dimensions are 42 mm × 21 mm × 8 mm.

(b) bases of $T_1$ and $T_2$ grounded through a $z_0$ resistor ($R_T = z_0$, no decoupling capacitor) for the integration of a positive voltage pulse.

## 6. Packaging in CAMAC and FASTBUS standards

Two standard ADC modules are currently under design. They are:

(a) A 32 channel single width CAMAC module.

(b) A 96 (possibly 128) channel single width FASTBUS module. It will be possible to operate these modules in a stand alone mode and the per channel cost should not exceed 60 SF for large quantities.

## 7. Conclusions

The circuits described in this paper are general purpose and the components have many equivalents. They can therefore safely be used in many applications.

Higher packaging densities may perhaps be achieved with an hybridized version of the circuit, however, the authors do not think that hybridization techniques would reduce the cost with respect to the present design.

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